## CLAIMS

What is claimed is:

1. A device comprising:

a first interface to first interconnect apparatus;

a second interface to second interconnect apparatus, the second interconnect apparatus of a type capable of connection to peripherals having direct memory access apparatus for transferring data;

the device capable of serving as a bridge for data transfer between the first interface and the second interface; and

address translation hardware coupled to translate I/O virtual addresses received from the second interface into physical memory addresses for transmission onto the first interface, the address translation hardware further comprising coherency maintenance apparatus.

2. The device of Claim 1, wherein the coherency maintenance apparatus maintains coherency by observing the first interface for references to entries of a page table in a memory.

3. The device of Claim 2 wherein a valid flag of the address translation hardware is altered when a memory reference having potential to modify a page entry table in memory is observed on the first interconnect apparatus and that page table entry in memory corresponds to an address mapping contained within the address translation hardware.

4 The device of Claim 1 wherein the mapping hardware is a translation lookaside buffer.

5. The device of Claim 4 wherein the coherency maintenance apparatus maintains coherency by observing the first interface for references to entries of a page table in a memory.

6. The device of Claim 4 wherein the coherency maintenance apparatus operates through a directory-based protocol.

7. A bridge comprising:

a first bus interface;

mapping hardware for translating an I/O virtual address into a physical memory address;

the mapping hardware coupled to transmit the physical memory address over the first bus interface;

wherein the mapping hardware has coherency maintenance apparatus associated therewith.

8. The bridge of Claim 7, wherein the coherency maintenance apparatus is capable of observing traffic on a bus coupled to the first bus interface, and altering address mappings stored in the mapping hardware in response to said traffic.

9. A computer system comprising at least one processor;

at least one memory system;

coupling apparatus, coupling the at least one processor and the at least one memory system;

at least one DMA-capable peripheral device coupled to the coupling apparatus;

at least one address translation apparatus, coupled to translate an I/O virtual address originating with the at least one DMA-capable peripheral device into a physical memory address, the address translation apparatus equipped with coherency maintenance apparatus, and the address translation apparatus is capable of transmitting the physical memory address to the at least one memory system.

10. The computer system of Claim 9, wherein the coupling apparatus couples to the at least one DMA-capable peripheral device through a host channel adapter and interconnect apparatus.

11. The computer system of Claim 9, wherein the coupling apparatus comprises a host bridge and an I/O bus.

12. The computer system of Claim 9, further comprising:

a second processor;

a second memory system;

a second host bridge, coupling the second processor and the second memory system to the system bus;

a second address translation apparatus, coupled to translate an I/O virtual address originating with the at least one DMA-capable peripheral device into a second physical memory address, the second address translation apparatus equipped

with coherency maintenance apparatus, and the second address translation apparatus equipped to transmit the second physical memory address to the second memory system.

13. The computer system of Claim 9, wherein there are at least two DMA-capable peripheral devices coupled to the coupling apparatus.

14. The computer system of Claim 9, wherein the at least one address translation apparatus further comprises a Translation Lookaside Buffer.

15. A computer system comprising

at least one processor;

at least one memory system;

at least one system controller, coupling the at least one processor and the at least one memory system to a host channel adapter;

at least one peripheral device coupled to the at least one host channel adapter;

at least one address translation apparatus, coupled to translate an I/O virtual address originating with the at least one peripheral device into a physical memory address, the address translation apparatus equipped with coherency maintenance apparatus, and the address translation apparatus equipped to transmit the physical memory address to the at least one memory system.

16. The computer system of Claim 15, wherein the coherency maintenance apparatus performs a snoop of addresses generated by the at least one processor.

17. The computer system of Claim 15, wherein the coherency maintenance apparatus is directory-based.

18. The computer system of Claim 17, wherein the coherency maintenance apparatus incorporates a cache directory.